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Fast and Accurate Moment LVF Characterization for Advanced Technology Nodes

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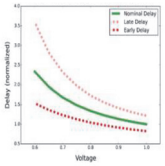
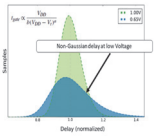
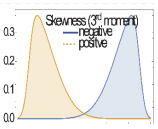
Abstract/Motivation

- **Advanced technology nodes use lower supply voltages to conserve power but this leads to high variability in the timing response of a chip**
  - Circuit delay is increasingly affected by process variations
  - Asymmetric distributions → long tails on late delays
  - Mean shift from nominal
  - The lower the voltage, the more non-Gaussian the distribution for arc delay
- **ULV corners requires the use of moment parameters in Liberty Variance Format (LVF) but this requires modeling the entire shape of the distribution which traditional methodology lacks in**
- **We propose a fast transistor level variance simulation in order to capture moment parameters accurately for use in advanced technology nodes**

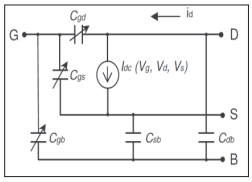






FX simulation model

- **Fast Transistor level (FX) timing model built for variance analysis[1)]**
- **FX model is very cheap to construct, as it is only concerned with individual transistor behaviors**
  - Generally well under 2 hours for a whole library, using only 8 cores
  - Model is valid for a wide voltage range, so model only needs to be constructed for each temperature and process corner and the bounding voltages
- **FX model captures the nominal behavior of each transistor *as well as* how that behavior changes under the influence of each variance parameter**
- **Cells are modeled as collections of FX transistors, together with all the RC devices present in the dspf extraction**
  - So all the RC interactions present in the SPICE model preserved, allowing for SPICE like accuracy



1) S.Raja, F.Varadi, M.Becer and J.Geada, "Transistor Level Gate Modeling for Accurate and Fast Timing, Noise and Power Analysis", in ICCAD, Electrical Cell Modeling Workshop, 2008

Moment LVF Validation Criteria

- **Comprehensive validation was performed on the new flow by comparison with Monte-Carlo SPICE for 100K samples**
- **Each moment LVF parameter from the new flow was validated against MC-SPICE result using the below equations:**
  - Means shift error needs to meet one of the following criteria

$$\text{Error} = \frac{\text{ABS}(MeanShift_{lib} - MeanShift_{MC})}{\text{ABS}(FixCornerValue) + 3\sigma_{MC} + MeanShift_{MC}} < 1\%$$
$$\text{Error} = \text{ABS}(MeanShift_{lib} - MeanShift_{MC}) < 1\text{ps}$$

  - Standard deviation needs to meet one of the following criteria

$$\text{Error} = \frac{3 \times \text{ABS}(\sigma_{lib} - \sigma_{MC})}{\text{ABS}(FixCornerValue) + 3\sigma_{MC}} < 3\%$$
$$\text{Error} = \text{ABS}(\sigma_{lib} - \sigma_{MC}) < 1\text{ps}$$

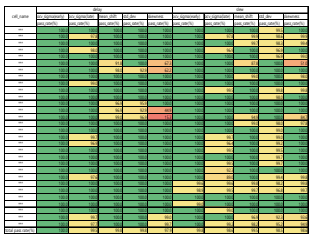
  - Skewness needs to meet one of the following criteria

$$\text{Error} = \frac{\text{ABS}(Skewness_{lib} - MeanShift_{MC})}{\text{ABS}(FixCornerValue) + 3\sigma_{MC}} < 3\%$$
$$\text{Error} = \text{ABS}(Skewness_{lib} - Skewness_{MC}) < 1\text{ps}$$

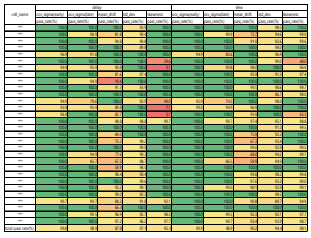
- **Validation was done at ultra-low-voltage corner for 7nm technology across 30 representative cells**

Moment LVF Validation Results

New FX Flow vs MCSpice QoR



Traditional Flow vs MCSpice QoR



- New FX flow provides superior QoR
- Traditional flow failed in many cells for moments
- FX flow provides faster runtime than traditional flow

** Cell names are hidden due to confidentiality reasons*

Runtimes	New FX methodology	Traditional methodology
Delay and Slew LVF	3.6hrs	8.3hrs

The new FX methodology provides superior runtime & QoR for LVF generation compared to the traditional methodology!

Summary

- **This work presented new approach of modeling variance using Fast Transistor (FX) modeling**
- **The proposed approach overcomes the limitations of traditional approach in modeling moment LVF parameters for ultra-low-voltage corners**
- **We performed comprehensive validation of the new proposed FX approach against MC-SPICE and found the QoR to meet our pass criteria for advanced products, while also providing fast turnaround time.**